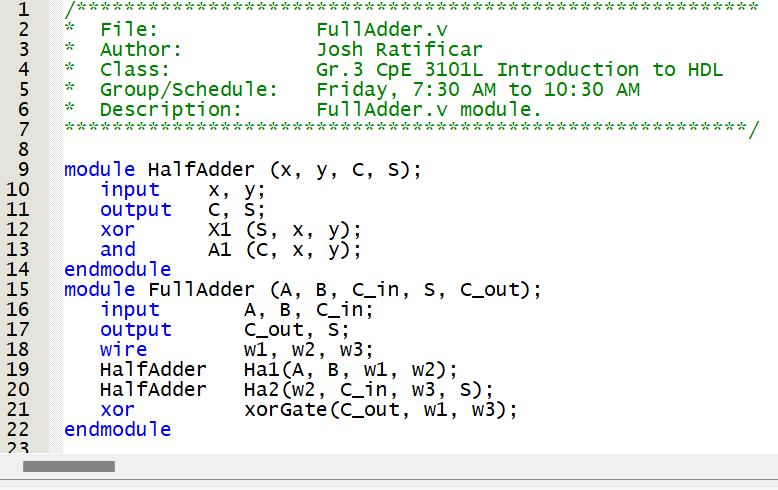
# Laboratory Report #2

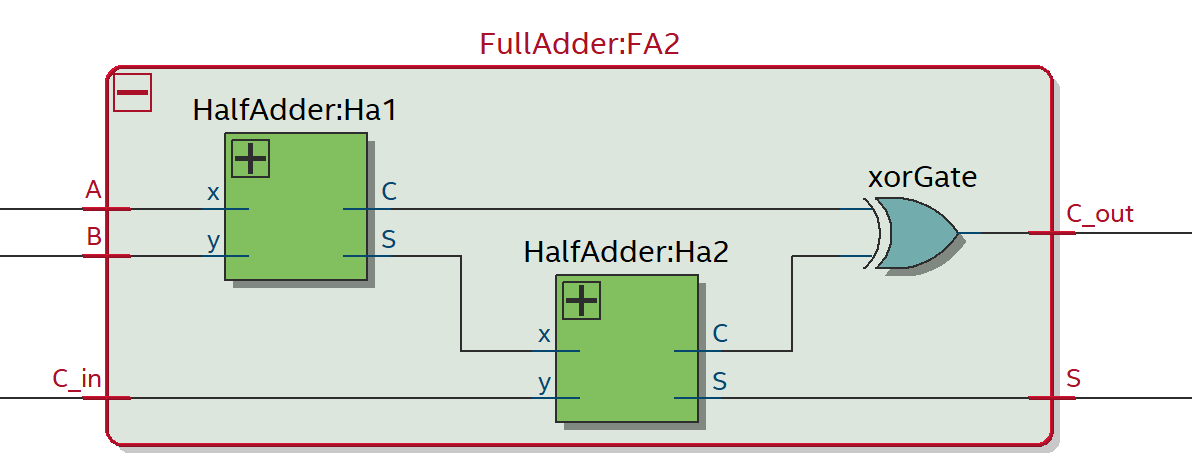
**Name:** Josh Ratificar **Date Completed:** 09-09-2023

**Laboratory Exercise Title:** Basic Constructs in Verilog HDL

**Part B.** *Full Adder*

****

**Figure 1.0 –** *Full Adder Module (with Half Adders)*

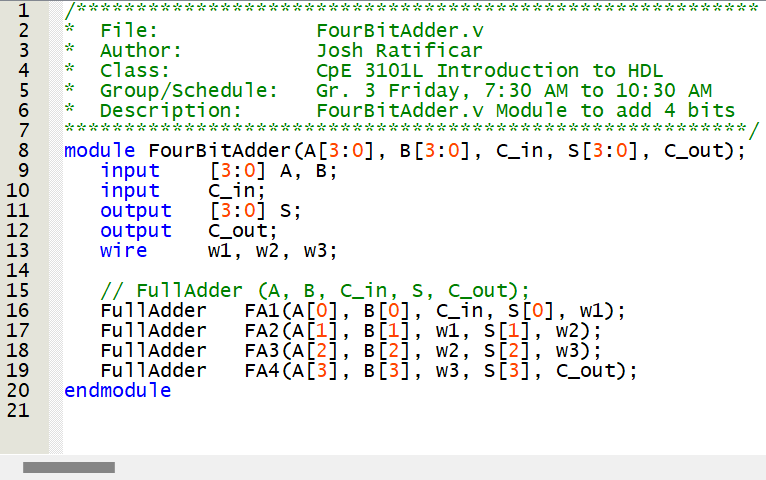
****

**Figure 1.1 *–*** *Full Adder**Block Diagram (RTL Viewer)*

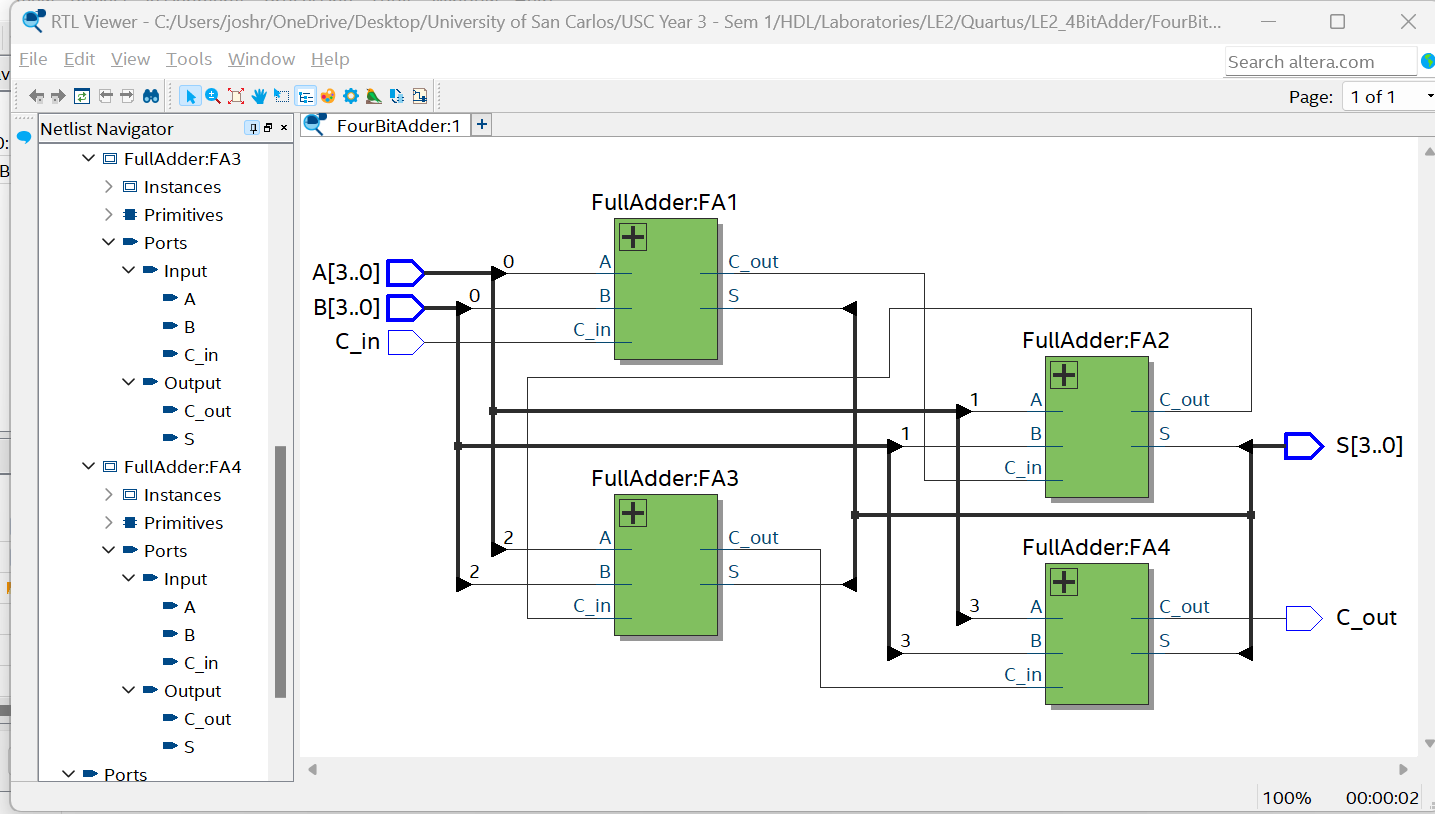
**Part C.** *Four-Bit Adder*

**Table. 2.0 –** *Compilation Report for Flow Summary*

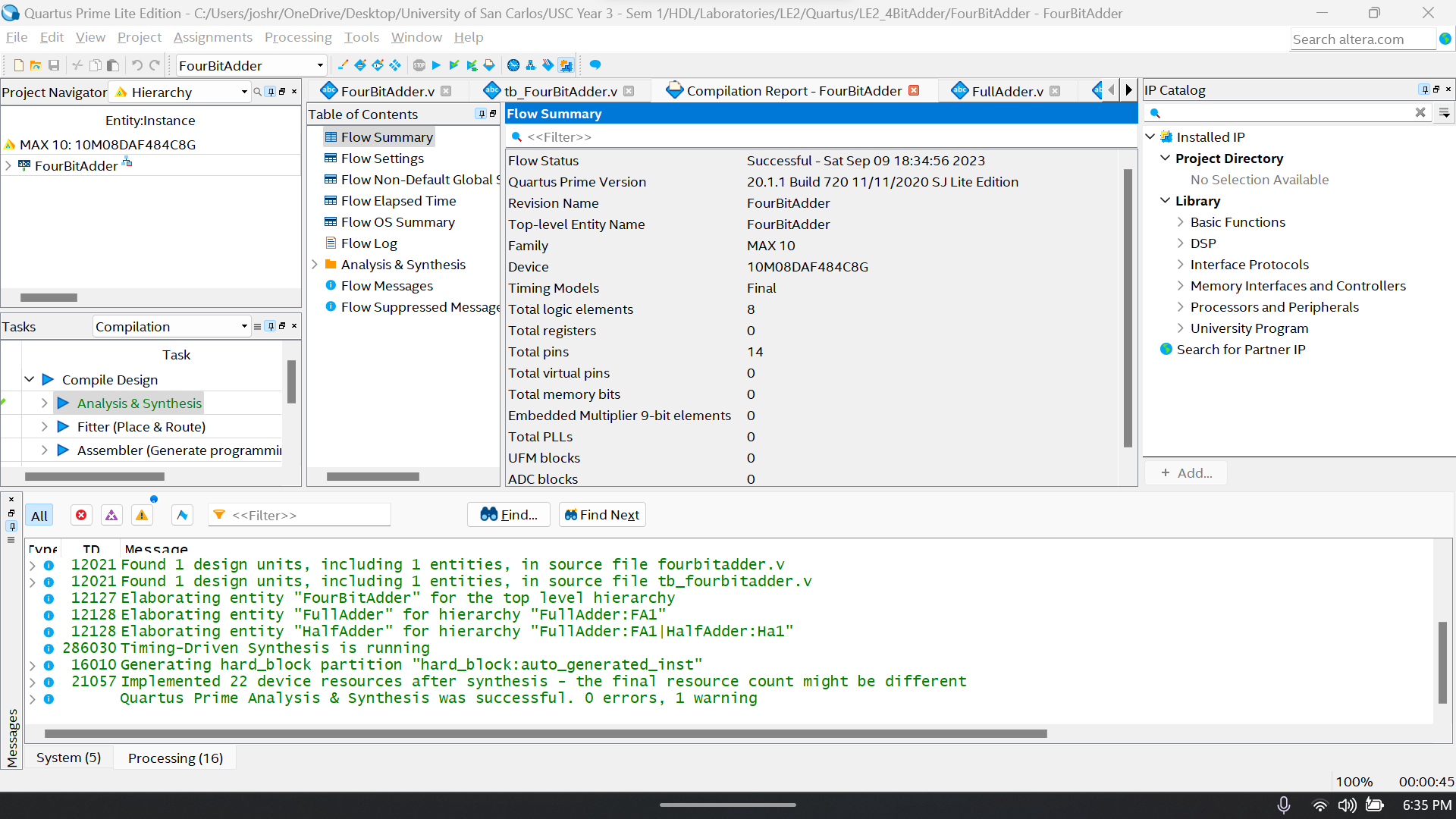
|  |  |
| --- | --- |
| # of Logic Elements Used: | 8 |
| # of Logic Pins Used: | **14** |

**

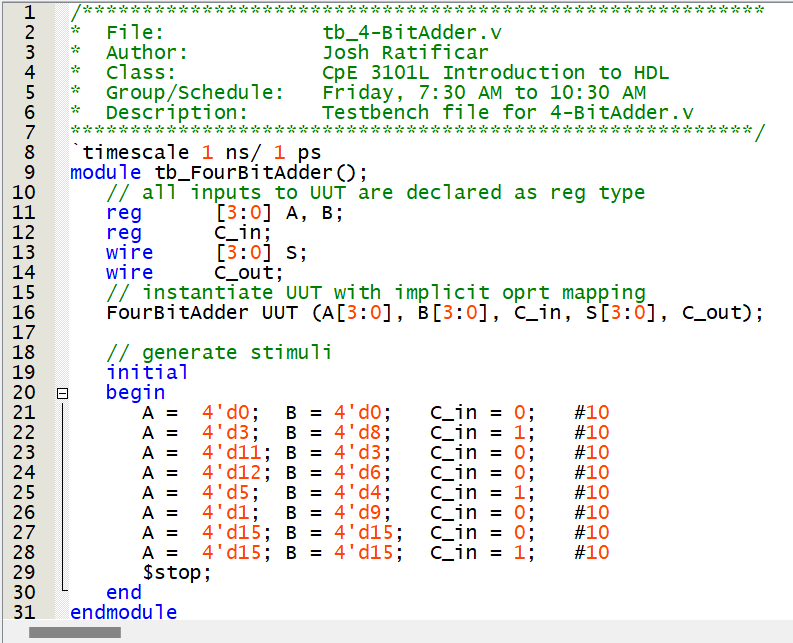
**Figure 2.0** – *FourBitAdder.v Module*

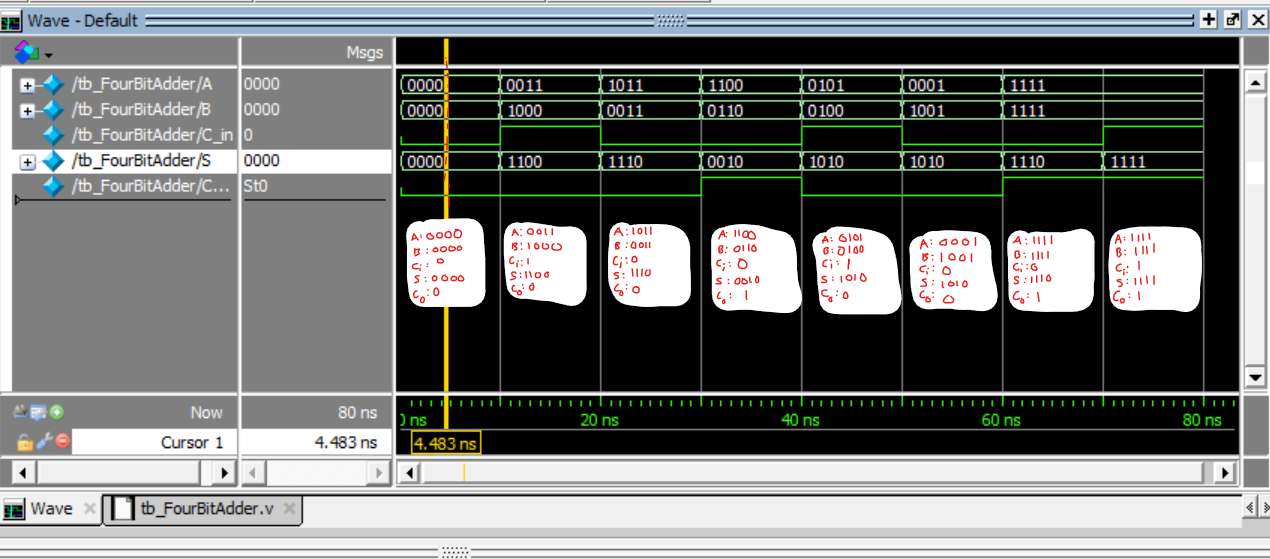
**

**Figure 2.0** – *FourBitAdder.v RTL Viewer*



**Figure 2.2** – *FourBitAdder.v Analysis and Synthesis*

**



**Figure 2.3** – *tb\_FourBitAdder.v Test Bench Script*

**Figure 2.4** – *tb\_FourBitAdder.v Test Bench Script*